Amendments to the Claims

1. (currently amended) A method for fabricating an integrated circuit, comprising the steps of:

forming a low-k dielectric layer over a semiconductor body;

forming a resist pattern over said low-k dielectric layer;

etching said low-k dielectric layer using said resist pattern; and

treating said low-k dielectric layer with a plasma having a bias power on the order of 400W, wherein said treating step occurs in-situ with respect to said etching step.

2. (original) The method of claim 1, wherein said plasma comprises O_2.

3. (original) The method of claim 1, wherein said plasma comprises H_2O.

4. (original) The method of claim 1, wherein said plasma comprises a gas selected from the group consisting of O_2, H_2, H_2O, H_2O_2, O_3, CO, CO_2, and SO_2.

5. (original) The method of claim 1, wherein said low-k dielectric layer comprises organo-silicate glass.

6. (original) The method of claim 1, wherein said low-k dielectric layer comprises an ultra-low-k dielectric layer having a dielectric constant less than 2.5.

7. (original) The method of claim 1, wherein said treating step removes said resist pattern.

8. (original) The method of claim 1, wherein said treating step occurs in the same chamber as the etching step.

9. (original) The method of claim 1, wherein said treating said occurs in a separate chamber of a tool used for the etching step.

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10. (original) The method of claim 9, wherein said low-k dielectric layer is transferred under vacuum from an etching chamber after said etching step to said separate chamber.

11. (currently amended) A method of fabricating an integrated circuit having copper metal interconnects, comprising the steps of:

forming an etchstop layer over a semiconductor body;

forming an interlevel dielectric (ILD) over the etchstop layer;

forming an intrametal dielectric (IMD) over the ILD;

forming a capping layer over said IMD

forming a via resist pattern over said capping layer;

etching a via in said IMD and ILD using said via resist pattern;

removing said via resist pattern using a plasma treatment to reduce poisoning by a nitrogen source, wherein said plasma treatment occurs in-situ with respect to said etching step and occurs under a bias power of approximately 400W;

at least partially filling said via with an organic material;

forming a trench resist pattern over said IMD;

etching a trench in said IMD using said trench resist pattern;

removing said trench resist pattern and said organic material in said via;

removing said capping layer and any exposed portion of the etchstop layer; and

forming a copper interconnect in said via and said trench.

12. (original) The method of claim 11, wherein said plasma treatment comprises O_2.

13. (original) The method of claim 11, wherein said plasma treatment comprises a gas selected from the group consisting of H_2, H_2O, H_2O_2, O_3, CO, CO_2, and SO_2.

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14. (original) The method of claim 11, wherein said plasma treatment occurs in the same chamber as the etching a via step.

15. (original) The method of claim 11, wherein said plasma treatment occurs in a separate chamber of the same tool as the etching a via step.

16. (new) A method for fabricating an integrated circuit, comprising the steps of:

forming a low-k dielectric layer over a semiconductor body;

forming a resist pattern over said low-k dielectric layer;

etching said low-k dielectric layer using said resist pattern; and

treating said low-k dielectric layer with a H_2 plasma to remove said resist pattern and reduce poisoning from a nitrogen source, wherein said treating step occurs in-situ with respect to said etching step.

17. (new) The method of claim 16, wherein said treating step removes said resist pattern.

18. (new) The method of claim 16, wherein said treating step occurs in the same chamber as the etching step.

19. (new) The method of claim 16, wherein said treating said occurs in a separate chamber of a tool used for the etching step.

20. (new) The method of claim 19, wherein said low-k dielectric layer is transferred under vacuum from an etching chamber after said etching step to said separate chamber.

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